

DDR, DDR2 and DDR3 Integrated Power Supply Controller

FEATURES

- DC-DC SMPS controller with integrated drivers for VDDQ
- Integrated Linear Regulator with 2A source and sink capability for VTT.
- High Efficiency up to 94%
- High light load efficiency; >85% at 100mA
- VDDQ accuracy $\pm 1\%$
- Input voltage from 3V to 30V
- Output voltage
 - Preset values at 2.5V or 1.8V or
 - adjustable from 0.5V to 2.75V
- Output current - up to 15A
- Power Good signal
- ON/SKIP signal
- Soft-Start and Soft-stop
- Voltage Feed-Forward Compensation
- Constant ripple-current control allows optimum inductor size
- Dynamic voltage change support
- Output Protection:
 - Latched Over Voltage Protection
 - Latched Under Voltage Protection
 - Valley type Over Current Protection
- Input Protection:
 - Under Voltage Lock Out on VDDA
 - Under Voltage Lock Out on VIN

APPLICATIONS

Power Supplies for DDR, DDR2 and DDR3 memory

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ812LN	0°C to 85°C	QFN24 (4x4mm) Lead-Free

GENERAL DESCRIPTION

OZ812 is a DC/DC controller specially developed to design power supplies for DDR, DDR2 and DDR3 memories. OZ812 steps down the high battery voltage to low output voltages in the range of 0.5V to 2.75V and also provides the memory reference VTTREF and termination voltage VTT that accurately tracks VDDQ/2. It is compliant with the DDR, DDR2 and DDR3 specifications.

Voltage Feed-Forward compensation assures high rejection of input voltage transients, typically occurring when the AC adapter is plugged in or removed.

Over Voltage Protection (OVP) acts when the output voltage exceeds the set voltage by more than 125mV. This protection condition is latched and initiates a ramp down of the output voltage.

Under Voltage Protection (UVP) acts when the output voltage falls below the set voltage by more than 133mV. This protection condition is latched and initiates a ramp down of the output voltage.

After an OVP or UVP event, the ON/SKIP pin should be toggled or VDDA/VIN cycled to restart the circuit.

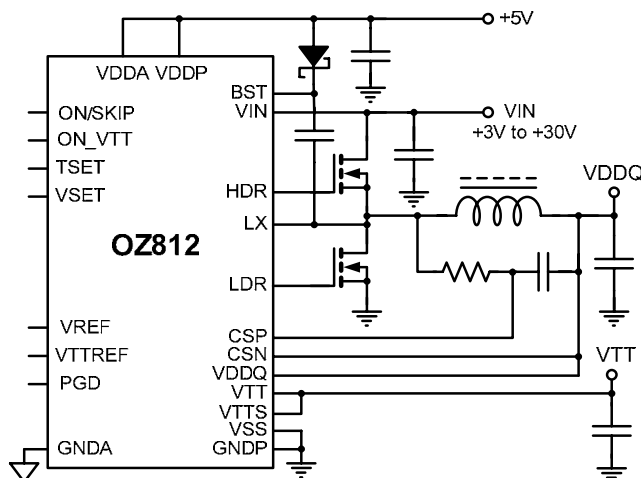
The DC/DC controller output is protected against overload by a valley current type, cycle-by-cycle Over Current Protection (OCP) circuit.

The Under Voltage Lock Out circuit monitors both, VDDA and VIN and lets the controller operate only if VDDA > 4.2V and VIN > 2.5V.

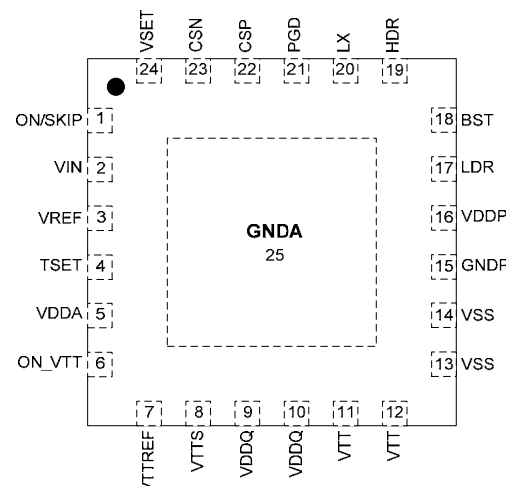
The Power Good signal is high as long as the output voltage is within +125mV/-133mV of the set voltage. At startup the output voltage ramps up in a controlled manner with a typical slew rate of 1V/ms (soft start) and at shutdown the output voltage is ramped down in a controlled manner with the same slew rate (soft stop).

VTTREF is able to source and sink 20mA tracking VDDQ/2 $\pm 1\%$. VTT tracks VREF within ± 40 mV and is able to source and sink 2A.

SIMPLIFIED APPLICATION DIAGRAM



PIN DIAGRAM



PIN DESCRIPTION

No.	Name	I/O	Type	Description
1	ON/SKIP	I	Digital	Enables DC/DC controller operation. If $V_{ON/SKIP} > 1V$, the Vout voltage ramps up to the voltage set on VSET pin with a slew rate of 1V/ms. If $V_{ON/SKIP} > 2.1V$ the controller enters skip mode of operation. If $V_{ON/SKIP} < 0.4V$ the chip is disabled and enters a very low consumption mode $< 1\mu A$.
2	VIN	I	Analog	Input voltage sense. Used for feed-forward compensation. Also monitored by the Under Voltage Lock Out circuit. Let the controller operate only if $V_{in} > 2.5V$.
3	VREF	O	Analog	2.75V +/- 1% precision reference voltage. A 0.1 μF capacitor should be placed from VREF to GNDA.
4	TSET	P	Power	Adjust the Ton of the controller according to the formula: $T_{on} = (1.6\mu s * V_{TSET}) / (V_{in} - V_{set})$ A 0.1 μF capacitor must be placed from TSET to GNDA.
5	VDDA	P	Power	+5V supply for the controller analog circuits. A 1 μF capacitor should be placed from VDDA to GNDA.
6	ON_VTT	I	Digital	Enables Linear Regulator operation while main controller is enabled. If $V_{ON_VTT} > 0.6V$, the VTT ramps up to the voltage on the VTTREF pin. If $V_{ON_VTT} < 0.4V$, VTT linear regulator enters a high impedance state.
7	VTTREF	O	Analog	VTTREF is CSN/2 able to source and sink up to 20mA.
8	VTTs	I	Analog	Linear Regulator sensing pin.
9	VDDQ	P	Power	Positive supply for the Linear Regulator. Connect to the output of the DC/DC regulator.
10	VDDQ	P	Power	Positive supply for the Linear Regulator. Connect to the output of the DC/DC regulator.
11	VTT	O	Analog	Output of the Linear Regulator
12	VTT	O	Analog	Output of the Linear Regulator
13	VSS	P	Power	Ground for the Linear Regulator
14	VSS	P	Power	Ground for the Linear Regulator
15	GNDP	P	Power	Power Ground.
16	VDDP	P	Power	Positive supply for the low side driver. A 1 μF capacitor should be placed from VDDP to GNDP.
17	LDR	O	Digital	Output of the low side driver
18	BST	P	Power	Positive supply for the high side driver. A 0.22 μF capacitor should be placed between BST and LX.
19	HDR	O	Digital	Output of the high side driver.
20	LX	P	Power	Inductor switching node.
21	PGD	O	Digital	Power Good output. It is an open drain output asserted high when the output voltage Vout is within +125mV/-133mV of the set value.
22	CSP	I	Analog	Non-inverting current sense pin.
23	CSN	I	Analog	Inverting current sense pin.
24	VSET	I	Analog	Sets the Vout output voltage. Uses a resistor divider from the reference voltage. If it is connected to GNDA the output voltage is regulated to 2.5V (DDR) If it is connected to VDDA the output voltage is regulated to 1.8V (DDR2)
25	GNDA	P	Power	Ground for the controller analog circuits.

BILL OF MATERIALS

Item	Qty	Reference	Value	Vendor	Part Number	PCB Footprint
1	1	CIN	2x10u/25V	TDK	C3225X5R1E106M	1210
2	1	COUT	2x220uF/6.3V	Sanyo	6TPD220M	D4D
3	2	C10, C11	47uF/6V	TDK	C3225X5R1E476M	1210
4	1	C3	0.1uF/10V	Any	Ceramic – X7R or X5R	0603
5	1	C6	0.22uF/10V	Any	Ceramic – X7R or X5R	0603
6	3	C1, C5, C13	1uF/10V	TDK	C1608X5R1A105K	0603
				Johanson Dielectrics	100R14X105M	
7	1	C2	10nF/25V	Any	Ceramic – X7R or X5R	0603
8	1	C7	3.3nF/25V	Any	Ceramic – X7R or X5R	0603
9	3	C4, C9, C12	1nF/6V	Any	Ceramic – X7R or X5R	0603
10	1	C8	22pF	Any	Ceramic	0603
11	1	R0	0	Any		0603
12	1	R1	22	Any		0603
13	1	R2	1k	Any		0603
14	1	R3	124k 1%	Any		0603
15	1	R4	150k 1%	Any		0603
16	1	R5	1k9	Any		0603
17	1	R6	100k 1%	Any		0603
18	2	R8, R9	51	Any		0603
19	1	D1	NONE	Vishay	MBR0540	SOD-123
20	1	D2	NONE	IR	15MQ040N	SMA
21	1	M1	NONE	Vishay	Si7892DP	PowerPAK
22	1	M2	NONE	Vishay	Si7336DP	PowerPAK
23	1	L1	1u/24A	Vishay	IHLP5050CERZ1R0M01	5050
24	1	U1	NONE	O2Micro, Inc.	OZ812	QFN24

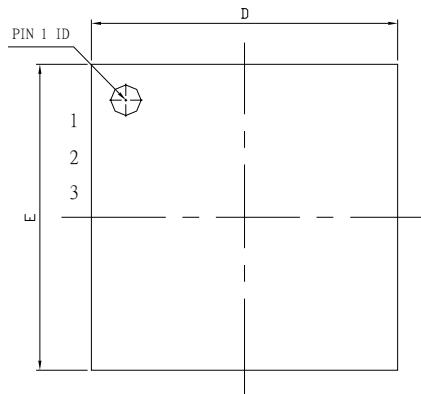
COMPONENT SUPPLIERS

Manufacturer	Contact Information	
	Phone	Website
Power MOSFETs		
Vishay	1-402-563-6866	www.vishay.com
Inductors		
Vishay	1-402-563-6866	www.vishay.com
Diode		
IR	1-303-283-7700	www.ir.com
Vishay	1-402-563-6866	www.vishay.com
Capacitors		
Vishay	1-847-803-6100	www.vishay.com
Johanson Dielectrics	1-818-364-9800	www.johansondielectrics.com
Sanyo	1-619-661-4134	www.sanyodevice.com
TDK	1-800-344-2112	www.tdk.com
Resistors		
Vishay	1-402-563-6866	www.vishay.com
TDK	1-800-344-2112	www.tdk.com

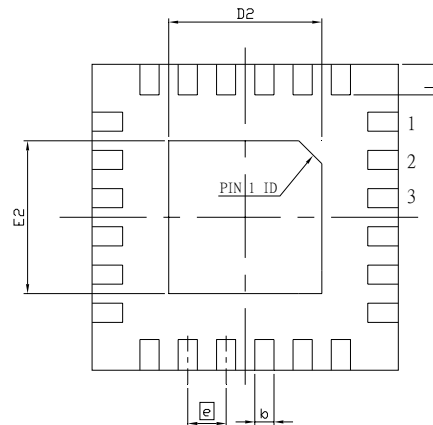
PACKAGE INFORMATION

Exposed pad is GNDA (pin 25) and must be fully soldered to PCB

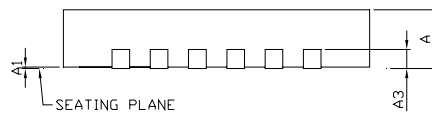
24Ld QFN 4x4mm Package Outline Drawing



TOP VIEW



BOTTOM VIEW



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e	0.50 BSC		
L	0.30	0.40	0.50

Notes:
1. ALL DIMENSIONS ARE IN MILLIMETER.

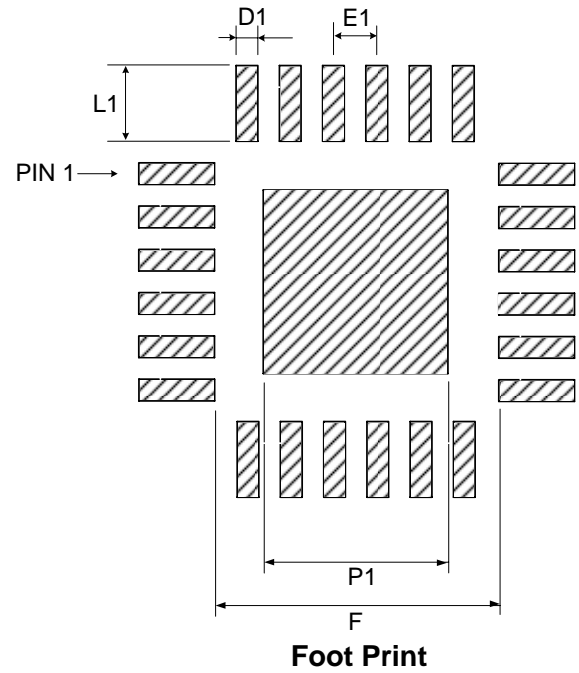
Rth j-a (QFN-24 4x4mm package) = 38°C/W

DIMENSION TABLE

SYMBOL	SPECIFICATION
	24L QFN 4X4 BODY
D1	0.25
E1	0.50
L1	0.80
P1	2.50
F	3.20

All dimensions are given in millimeters.

RECOMMENDED LANDING PATTERN



PACKAGE MARKING (QFN24 PACKAGE)

812LN

Mark	Function
N	Lead-Free Package

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